Assignment 1, Part B

1. (20%) A computer has a word-addressable (not byte-addressable) memory consisting of 1M 16-bit words. It also has a 4K-word cache that is 4-way set associative and in which there are 64 words per block.

   (a) Calculate the number of bits in the tag, set index, and block offset fields of the memory address.

   (b) Assume that the cache is initially empty. Suppose that the processor fetches 4352 words from locations 0, 1, 2, ..., 4351 in that order. It then repeats this fetch sequence nine more times. If the cache is ten times faster than the main memory, what is the improvement factor (the speed-up) resulting from the use of the cache, assuming that the LRU algorithm is used for block replacement?

2. (20%) A machine has a virtual address space with 32-bit byte addresses, a 2 KB page size and 128 MB of physical memory. Draw a diagram showing how a virtual address in this machine is translated into a physical address, assuming that the MMU has an 8-entry fully associative TLB. Label all lines and show how many bits are in each part.

3. (10%) A machine has a 32-bit virtual address space and a 16KB page size. It has 1GB of physical memory. How many pages does a process have? How many bytes are needed for a page table, assuming 4 control bits and that disk addresses are stored elsewhere?