



Sample Midterm Exam Questions

1. Suppose a computer has a 4-way set associative cache with one-word blocks. It has a capacity of 256 bytes. Given the sequence of byte addresses 8, 64, 96, 128, 64, 96, 256, 192, 24 show the final cache contents and state the number of hits and misses.

The block addresses for this sequence are 2, 16, 24, 32, 16, 24, 64, 48, 6. There are $256/(4*4) = 16$ sets. Therefore, the mapping of block address to sets is $\text{block_addr} \% 16$. The sequence generates the following table. Empty sets are not shown. The currently accessed cache block is in boldface. The notation $m[i]$ means the word located at memory address i .

byte #	block #	set #		set0	set0	set0	set0	set2	set6	set8
				block0	block1	block2	block3	block0	block0	block0
8	2	2	miss					m[8]		
64	16	0	miss	m[64]				m[8]		
96	24	8	miss	m[64]				m[8]		m[96]
128	32	0	miss	m[64]	m[128]			m[8]		m[96]
64	16	0	hit	m[64]	m[128]			m[8]		m[96]
96	24	8	hit	m[64]	m[128]			m[8]		m[96]
256	64	0	miss	m[64]	m[128]	m[256]		m[8]		m[96]
192	48	0	miss	m[64]	m[128]	m[256]	m[192]	m[8]		m[96]
24	6	6	miss	m[64]	m[128]	m[256]	m[192]	m[8]	m[24]	m[96]

There were 7 misses and 2 hits.

2. A machine has a base CPI of 2 clock cycles. Measurements obtained show that the instruction miss rate is 12% and the data miss rate is 6%, and that on average, 30% of all instructions contain one data reference. The miss penalty for the cache is 10 cycles. What is the total CPI?

$$\begin{aligned}
 \text{Effective CPI} &= 2.0 + \text{instruction miss cycles} + \text{data miss cycles} \\
 &= 2.0 + 0.12*10 + 0.30*0.06*10 = 2.0 + 1.2 + 0.18 \\
 &= 3.38
 \end{aligned}$$

3. A machine has a 500MHz system clock. Memory takes 30 ns to access a word. How many clock cycles is this?

$$\begin{aligned}
 &\text{Clock cycles to access a word} \\
 &= 30 \text{ ns} / (1 \text{ clock cycle}) * (500 * 10^6 \text{ clock cycles/sec}) * (1 \text{ sec} / 10^9 \text{ ns}) \\
 &= 30 * 500 * 10^{-6} * 10^{-9} \\
 &= 15000 * 10^{-3} = 15 \text{ clock cycles}
 \end{aligned}$$

4. A machine has a 32-bit virtual address space and a 16KB page size. It has 1GB of physical memory. How many pages does a process have? How many bytes are needed for a page table, assuming 4 control bits and that disk addresses are stored elsewhere?

$$\begin{aligned}
 \text{Pages per process} &= 2^{32} \text{ bytes} * (1 \text{ page} / 16*2^{10} \text{ bytes}) = 2^{32} / 2^{14} \\
 &= 2^{18} = 256K \text{ pages}
 \end{aligned}$$

5. A machine with a two level cache has a base CPI of 1.5 when all references hit the primary cache. Given the following characteristics:

- a clock rate of 250MHz
- memory access time of 100ns

- miss rate at the primary cache of 5%
- secondary cache access time of 10ns
- miss rate at secondary cache of 1%

what is the total CPI?

The clock rate of 250 MHz implies a clock cycle of length 4 ns (because $1/(250 \cdot 10^6) = 4 \cdot 10^{-9}$). Therefore the memory access time is 25 cycles and the secondary cache access time is 2.5 cycles.

$$\begin{aligned} \text{The effective CPI} &= 1.5 + \text{cycles missed by primary but caught by secondary} \\ &\quad + \text{cycles missed by both caches} \\ &= 1.5 + (0.05 - 0.01) \cdot 2.5 + 0.01 \cdot (2.5 + 25) \\ &= 1.5 + 0.1 + 0.275 = 1.875 \end{aligned}$$

6. Draw a picture showing the organization of a direct-mapped cache with 16 words per block, with a capacity of 128KB. Show any multiplexors, gates, needed. Show how a 32-bit physical address is mapped to a cache block.

Cache capacity is 128KB. Each block has $16 \cdot 4 = 64$ bytes. There are $128K/64 = 2K = 2048$ blocks. The bytes offset is 2 bits, the word offset is 4 bits ($16 = 2^4$) and the index is 11 bits since $2K = 2^{11}$. That leaves 15 bits for the tag.

